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EXAMINER	
WILSON, JACQUELINE B	

ART UNIT	PAPER NUMBER
2612	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,609	MEAD ET AL.	
	Examiner	Art Unit	
	Jacqueline Wilson	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/13/03, 12/11/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: *IDS 07/19/02,05/06/02*.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 10, 11, 30, 31, 40, 41, 62, 63 and 67 are rejected under 35 U.S.C. 102(e) as being anticipated by Parulski et al (US 6,292,218).

Regarding Claim 1, Parulski et al teaches a lens system (22), a semiconductor sensor array (20) located on the optical axis at the focal place of the lens system (see fig. 2), the semiconductor sensor array having a plurality of pixels (see fig. 3A, element 66), each of the pixels generating an output signal that is a function of light incident thereon (col. 3, lines 41+), a sensor control circuit (timing and control section 27 and sensor timing circuit 28) coupled to the semiconductor sensor array and adapted to produce sensor control signals for controlling an operation of the pixels in the semiconductor sensor array in response to input from a user of the camera system (col. 3, lines 48+), an addressing circuit (27 and sensor timing circuit 30) coupled to the semiconductor sensor array and configured to produce a first set of image output signals (referred to as higher quality still mode) and a second set of image output

signals (referred to as low quality motion mode; col. 4, lines 35+) from the semiconductor sensor array, the first set of image output signals being indicative of an intensity of the light at a first set of the pixels when the sensor control signals are in a first state (still mode), the second set of image output signals being indicative of an intensity of the light at a second set of the pixels when the sensor control signals are in a second state (motion mode), the first set of pixels including more pixels than the second set of pixels (col. 6, lines 29-50), a storage medium (26) adapted to store a representation of the first set of image output signal when the sensor control signals are in the first state (col. 6, lines 64- col. 7, line 4), and a display (10) adapted for displaying the second set of image output signals when the sensor control signals are in the second state (col. 7, lines 8-40).

Regarding Claim 2, Parulski et al teaches the first set of pixels is a majority of the pixels in the array (fig. 5 shows all lines of the sensor read out; col. 6, lines 64+) and the second set of pixels is a preset fraction (col. 7, lines 17+ teaches the first two line are read out, the next two lines are eliminated, the following two lines are read out, the next four lines are eliminated, and repeats until the pixels are readout). This teaches that the preset fraction of the pixels in the array is less than half of a total of the pixels in the array.

Claim 10 is analyzed and discussed with respect to Claim 1. Furthermore, Parulski et al teaches a means for computing focus signals (via image statistics circuit 60) indicating a quality of focus of the light from the image output signal when the sensor control signals are in the second state (preview mode is performed in the motion

mode of image capture as disclosed in col. 4, lines 18-40) and for generating lens control signals in response to the focus signals (via lens motor drivers 50), and focusing control means in the lens system responsive to the lens control signals (via focus motor 46).

Claim 11 is analyzed and discussed with respect to Claim 2. (See rejection of Claim 2 above.)

Regarding Claim 30, Parulski et al teaches a lens system (22), a semiconductor sensor array (20) optically coupled to the lens system (see fig. 2), the semiconductor sensor array having a plurality of pixels arranged in a plurality of row and columns (see fig. 3A, element 66), each of the pixels generating an output signal that is a function of light incident thereon (col. 3, lines 41+), an addressing circuit (30) associated with the semiconductor sensor array, the addressing circuit having a storage addressing mode for generating storage addressing signals to the semiconductor sensor array in which substantially all of the rows and columns of the pixels in the array are addressed (col. 6, lines 29+), and a display addressing mode for generating display addressing signal to the semiconductor sensor array in which substantially less than all of the rows and columns of the pixels in the array are addressed (58; col. 4, lines 38+ and col. 7, lines 7+), a sensor control circuit (timing and control section 27 and sensor timing circuit 28) coupled to the semiconductor sensor array and to the addressing circuit and operable to produce sensor control signals and addressing signals addressing circuit control signals for controlling an operation of the pixels in the semiconductor sensor array in response to input from a user of the camera system (col. 3, lines 48- col. 4), a storage medium

(26) coupled to the semiconductor sensor array and operable to store data representing an image sensed by the semiconductor sensor array and presented to the storage medium from the semiconductor sensor array in response to the storage addressing signal (col. 6, lines 64- col. 7, line 4), and a display (10) coupled to the semiconductor sensor array (see fig. 2) and operable to display data representing an image sensed by the semiconductor sensor array and presented to the display from the semiconductor sensor array in response to the display addressing signals (col. 7, lines 8-40).

Claim 31 is analyzed and discussed with respect to Claim 2. (See rejection of Claim 2 above.)

Claim 40 is analyzed and discussed with respect to Claim 30. Furthermore, Parulski et al teaches a focus-signal computing circuit configured to receive the display data from the semiconductor sensor array in response to the display addressing signals (output from A/D converter 34) and to compute focus signals (via image statistics circuit 60) indicating a quality of focus of the image and for generating lens control signals in response to the focus signal (via lens motor drivers 50), and focusing control apparatus in the lens system coupled to and responsive to the lens control signals (via focus motor 46).

Claim 41 is analyzed and discussed with respect to Claim 2. (See rejection of Claim 2 above.)

Regarding Claim 62, Parulski et al teaches placing an image on a semiconductor sensor array (20) having a plurality of rows and columns (see fig. 3A) of pixel sensors disposed thereon, addressing a first group of the pixels on the semiconductor sensor

array, the first group of pixels comprising substantially less than all of the row and columns of the pixels in the array to obtain display data (referred to as motion mode; col.6, lines 32+), displaying the display data on a display (LCD 10) associated with the electronic camera, sensing an image-capture request made by a user (referred to as still mode; col. 6, line 29), and addressing a second group of pixels on the semiconductor sensor array, the second group of the pixels comprising substantially all of the row and columns of the pixels in the array to obtain image-storage data (col. 6, lines 29-31), and storing the image-storage data in a storage medium associated with the electronic camera data in response to the image-capture request (col. 6, lines 64-col. 7, line 4).

Regarding Claim 63, Parulski et al teaches addressing the first group of the pixels on the semiconductor sensor array comprises addressing selected ones of the rows and columns of the pixels on the semiconductor sensor array (col. 7, lines 8-40), and addressing the second group of the pixels on the semiconductor sensor array comprises addressing substantially all of the rows and columns of the pixels on the semiconductor sensor array (col. 6, lines 28+).

Regarding Claim 67, Parulski et al teaches computing a focus metric from the display data (using image statistics 60 for computing various "measurements" including adjusting focus; col. 4, lines 18-41), and adjusting a focus of the image on the semiconductor sensor array (via lens) in response to the focus metric (col. 4, lines 6-18).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4, 12, 13, 32, 33, 34, 42-44, and 64-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al (US 6,292,218) in view of Koseki et al (US 6,204,879).

Regarding Claims 3 and 4, Parulski et al teaches the array is arranged as a plurality of rows and columns of pixels (as shown in fig. 3A), but fails to specifically teach the second set of pixels comprises pixels from not more than half of the rows and not more than half of the columns of the array, wherein not more than half of the rows includes every Nth row and not more than half of the columns includes every Nth column, N is an integer greater than one. However, Koseki et al teaches that it is notoriously well known in the art to use a thinning-out scan driving means to read out every 4th pixel in both the lengthwise (column) and sideways (row) so as to extract specific pixels or outputting the pixels in a partial area within the whole image area (col. 6, lines 35+ and col. 7, lines 55+). This allows not more than half of the rows and not more than half of the columns to be read out. By thinning out the pixels of the image sensor provides a signal to a display conforming to the display system (i.e. NTSC). Therefore it would have been obvious to one having ordinary skill in the art to have the

second set of pixels comprises pixels from not more than half of the rows and not more than half of the columns of the array, wherein not more than half of the rows includes every Nth row and not more than half of the columns includes every Nth column, N is an integer greater than one.

Claims 12 and 13 are analyzed and discussed with respect to Claims 3 and 4. (See rejection of Claims 3 and 4 above.)

Claims 32-34 are analyzed and discussed with respect to Claims 3 and 4. (See rejection of Claims 3 and 4 above.)

Claims 42-44 are analyzed and discussed with respect to Claims 3 and 4. (See rejection of Claims 3 and 4 above.)

Claims 64-66 are analyzed and discussed with respect to Claims 3 and 4. (See rejection of Claims 3 and 4 above.)

5. Claims 5-9, 14-18, 35-39, and 47-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al (US 6,292,218) in view of Jacobs (US 6,580,456).

Regarding Claims 5 and 6, although Parulski et al teaches a color sensor array, Parulski et al fails to specifically disclose the semiconductor sensor array is a CMOS sensor array, which is a vertical color filter CMOS sensor array. However, Jacobs teaches a programmable timing generator for an image sensor that is either a CCD or a CMOS device (col. 3, lines 13+) for selectively outputting pixels in the sensor (col. 2, lines 16+). Using either CCD or CMOS technology is notoriously well known in the art

as alternative ways for capturing images. Jacobs further teaches that the image sensor has a geometric arrangement of cells including three colors (col. 5, lines 24+) for color imaging. It is inherent that the color arrangement is set to complement the sensor array (horizontally and vertically), and therefore is deemed inherent that a "vertical" color filter is used in the image sensor. One having ordinary skill would recognize that using the vertical color filter CMOS sensor array in the Parulski et al camera is an alternate method of capturing color image signals. Therefore, it would have been obvious to one having ordinary skill in the art to use a CMOS sensor array, which is a vertical color filter CMOS sensor array for capturing images.

Regarding Claims 7, 8, and 9, although a removable memory card is disclosed, Parulski et al fails to teach the storage medium is a semiconductor memory array, a magnetic disk storage device, or an optical disk storage device. However, Jacobs teaches a storage device (110) may be numerous devices such as a tape drive, a disk drive such floppy disk drive, hard disk drive, optical disk drive or magneto-optical disk drive, or an integrated circuit card or chip with RAM or EEPROM (col. 3, lines 23-27). These devices are notoriously well known in the art for storing images. It would have been obvious to use any one of these devices, for they serve the same purpose of maintaining images. Therefore, it would have been obvious to one having ordinary skill in the art to modify Parulski et al by using a semiconductor memory array, a magnetic disk storage device, or an optical disk storage device as taught in Jacobs for the purpose of storing images captured by the camera.

Claims 14 and 15 are analyzed and discussed with respect to Claims 5-6. (See rejection of Claims 5-6 above.)

Claims 16-18 are analyzed and discussed with respect to Claims 7-9. (See rejection of Claims 7-9 above.)

Claims 35 and 36 are analyzed and discussed with respect to Claims 5-6. (See rejection of Claims 5-6 above.)

Claims 37-39 are analyzed and discussed with respect to Claims 7-9. (See rejection of Claims 7-9 above.)

Claims 47-49 are analyzed and discussed with respect to Claims 7-9. (See rejection of Claims 7-9 above.)

6. Claims 19, 20, 21, 22, 25, 50, 51, 52, 53, 57, and 68-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al in view of Chung et al (US 6,677,996).

Regarding Claim 19, Parulski et al teaches a lens system (22) a semiconductor sensor array (20) having a plurality of pixels (fig. 3A, 66), each of the pixels generating an output signal that is a function of integration during an integration time (inherent in the system since exposure is performed) of a signal that is a function of light incident thereon, a sensor control circuit (timing and control section 27 and sensor timing circuit 28) coupled to the semiconductor sensor array and adapted to produce sensor control signals for controlling an operation of the pixels in the semiconductor sensor array in response to input from a user of the camera system (col. 3, lines 48+), an addressing

circuit (27 and sensor timing circuit 30) coupled to the semiconductor sensor array and configured to produce a first set of image output signals (referred to as higher quality still mode) and a second set of image output signals (referred to as low quality motion mode; col. 4, lines 35+) from the semiconductor sensor array, the first set of image output signals being indicative of an intensity of the light at a first set of the pixels when the sensor control signals are in a first state (still mode), the second set of image output signals being indicative of an intensity of the light at a second set of the pixels when the sensor control signals are in a second state (motion mode), the first set of pixels including more pixels than the second set of pixels (col. 6, lines 29-50), a storage medium (26) adapted to store a representation of the first set of image output signal when the sensor control signals are in the first state (col. 6, lines 64- col. 7, line 4), a display (10) adapted for displaying the second set of image output signals when the sensor control signals are in the second state (col. 7, lines 8-40), an exposure detection means (27) and exposure control means (27/52 provides timing signals for operating the sensor) for terminating the integration period of the sensor (inherent in the system since images are captured such that a beginning and end of integration is performed). However, Parulski et al fails to specifically disclose the exposure detection means generates an overall exposure signal indicating an aggregate state of exposure of the pixels during the integration time when the sensor control signals are in the first state and the exposure control means terminates the integration period in response to the overall exposure signal. In the same field of endeavor, Chung et al teaches optimizing light exposure by terminating the light exposure of a CMOS imager when instantaneous

aggregate pixel current falls below a preset level (col. 6, lines 44-47). Chung et al discloses detecting exposure such that by aggregating currents of selected pixels, the amount of light falling on the entire imaging surface is used to trigger the control signal for terminating the light exposure (col. 7, lines 38-42). Better control over the light exposure of the imaging surface is attained since the amount of incident light of a field of pixels, rather than a single pixel, is used (col. 6, lines 48-52). Although Parulski et al teaches a CCD sensor, one having ordinary skill in the art would recognize that esing either CCD or CMOS technology is notoriously well known in the art as alternative ways for capturing images. Modifying Parulski et al with the CMOS sensor of Chung et al does not change the scope of the invention by merely using a different type of device for performing the same function. Therefore, it would have been obvious to one having ordinary skill in the art to have the exposure detection means generate an overall exposure signal indicating an aggregate state of exposure of the pixels during the integration time when the sensor control signals are in the first state and the exposure control means terminates the integration period in response to the overall exposure signal.

Regarding Claim 20, Parulski et al teaches a flash illumination source (18) coupled to the sensor control circuit to be enabled in response to user input (col. 3, lines 36-40). However, Parulski et al fails to specifically disclose disabling a flash in response to the overall exposure signal. It would have been obvious to one having ordinary skill in the art to disable a flash in response to an overall exposure signal to restrict excess light from saturating the image sensor. Parulski et al teaches that upon

activating the capture button (16), the firing of the flash when necessary is used when ambient light is insufficient for capturing a still image (col. 3, lines 36+). In this case, if the overall exposure signal has adequate ambient light, one having ordinary would recognize that a flash would be unnecessary, therefore disabling the flash. Therefore, it would have been obvious to one having ordinary skill in the art to disable a flash in response to the overall exposure signal, such that excessive light may be reduced.

Claim 21 is analyzed and discussed with respect to Claim 10. (See rejection of Claim 10 above.)

Claim 22 is analyzed and discussed with respect to Claim 2. (See rejection of Claim 2 above.)

Claim 25 is analyzed and discussed with respect to Claim 19. (See rejection of Claim 19 above.)

Claim 50 is analyzed and discussed with respect to Claim 19. (See rejection of Claim 19 above.)

Claim 51 is analyzed and discussed with respect to Claim 20. (See rejection of Claim 20 above.)

Claim 52 is analyzed and discussed with respect to Claim 10. (See rejection of Claim 10 above.)

Claim 53 is analyzed and discussed with respect to Claim 2. (See rejection of Claim 2 above.)

Claim 57 is analyzed and discussed with respect to Claim 19. (See rejection of Claim 19 above.)

Claim 68 is a method claim of Claim 19 and is therefore analyzed and discussed. (See rejection of Claim 19 above.)

Claim 69 is analyzed and discussed with respect to Claim 20. (See rejection of Claim 20 above.)

7. Claims 23, 24, 54 and 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al, Chung et al (US 6,677,996), and in further view of Koseki et al (US 6,204,879).

Regarding Claims 23 and 24, Parulski et al teaches the array is arranged as a plurality of rows and columns of pixels (as shown in fig. 3A), but fails to specifically teach the second set of pixels comprises pixels from not more than half of the rows and not more than half of the columns of the array, wherein not more than half of the rows includes every Nth row and not more than half of the columns includes every Nth column, N is an integer greater than one. However, Koseki et al teaches that it is notoriously well known in the art to use a thinning-out scan driving means to read out every 4^{th} pixel in both the lengthwise (column) and sideways (row) so as to extract specific pixels or outputting the pixels in a partial area within the whole image area (col. 6, lines 35+ and col. 7, lines 55+). This allows not more than half of the rows and not more than half of the columns to be read out. By thinning out the pixels of the image sensor provides a signal to a display conforming to the display system (i.e. NTSC). Therefore it would have been obvious to one having ordinary skill in the art to have the second set of pixels comprises pixels from not more than half of the rows and not more

than half of the columns of the array, wherein not more than half of the rows includes every Nth row and not more than half of the columns includes every Nth column, N is an integer greater than one.

Claims 54-56 are analyzed and discussed with respect to Claims 23 and 24. (See rejection of Claims 23 and 24 above.)

8. Claims 26-29, and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al, Chung et al (US 6,677,996) and in view of Jacobs (US 6,580,456).

Regarding Claim 26, although Parulski et al teaches a color sensor array, Parulski et al fails to specifically disclose the semiconductor sensor array is a vertical color filter CMOS sensor array. However, Jacobs teaches a programmable timing generator for an image sensor that is either a CCD or a CMOS device (col. 3, lines 13+) for selectively outputting pixels in the sensor (col. 2, lines 16+). Using either CCD or CMOS technology is notoriously well known in the art as alternative ways for capturing images. Jacobs further teaches that the image sensor has a geometric arrangement of cells including three colors (col. 5, lines 24+) for color imaging. It is inherent that the color arrangement is set to complement the sensor array (horizontally and vertically), and therefore is deemed inherent that a "vertical" color filter is used in the image sensor. One having ordinary skill would recognize that using the vertical color filter CMOS sensor array in the Parulski et al camera is an alternate method of capturing color

image signals. Therefore, it would have been obvious to one having ordinary skill in the art to use a vertical color filter CMOS sensor array for capturing images.

Regarding Claims 27-29, although a removable memory card is disclosed, Parulski et al fails to teach the storage medium is a semiconductor memory array, a magnetic disk storage device, or an optical disk storage device. However, Jacobs teaches a storage device (110) may be numerous devices such as a tape drive, a disk drive such floppy disk drive, hard disk drive, optical disk drive or magneto-optical disk drive, or an integrated circuit card or chip with RAM or EEPROM (col. 3, lines 23-27). These devices are notoriously well known in the art for storing images. It would have been obvious to use any one of these devices, for they serve the same purpose of maintaining images. Therefore, it would have been obvious to one having ordinary skill in the art to modify Parulski et al by using a semiconductor memory array, a magnetic disk storage device, or an optical disk storage device as taught in Jacobs for the purpose of storing images captured by the camera.

Claim 58 is analyzed and discussed with respect to Claim 26. (See rejection of Claim 26 above.)

Claims 59-61 are analyzed and discussed with respect to Claim 27-29. (See rejection of Claim 27-29 above.)

9. **Claims 45 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parulski et al (US 6,292,218), Koseki et al (US 6,204,879), and in view of Jacobs (US 6,580,456).**

Regarding Claims 45 and 46, although Parulski et al teaches a color sensor array, Parulski et al fails to specifically disclose the semiconductor sensor array is a CMOS sensor array, which is a vertical color filter CMOS sensor array. However, Jacobs teaches a programmable timing generator for an image sensor that is either a CCD or a CMOS device (col. 3, lines 13+) for selectively outputting pixels in the sensor (col. 2, lines 16+). Using either CCD or CMOS technology is notoriously well known in the art as alternative ways for capturing images. Jacobs further teaches that the image sensor has a geometric arrangement of cells including three colors (col. 5, lines 24+) for color imaging. It is inherent that the color arrangement is set to complement the sensor array (horizontally and vertically), and therefore is deemed inherent that a "vertical" color filter is used in the image sensor. One having ordinary skill would recognize that using the vertical color filter CMOS sensor array in the Parulski et al camera is an alternate method of capturing color image signals. Therefore, it would have been obvious to one having ordinary skill in the art to use a CMOS sensor array, which is a vertical color filter CMOS sensor array for capturing images.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacqueline Wilson whose telephone number is (571) 272-7322. The examiner can normally be reached on 8:30am-5:00pm (alternate Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JW
04/15/05

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